What is claimed is:

1. A processor having a reconfigurable field of data processing cells and a register means,
wherein the register means has a data stream memory means designed to store a data stream and/or parts thereof.

2. The processor as recited in the preceding claim,
wherein a register means allocation means and/or a register means releasing means is provided.

3. The processor as recited in one of the preceding claims,
wherein the register allocation means is designed to be preserved over multiple reconfigurations.

4. The processor as recited in one of the preceding claims,
wherein a RAM PAE, optionally modified, is provided as the register means.

5. The processor as recited in one of the preceding claims,
wherein register means designed for reading and writing access are provided, in particular when a virtual FIFO dividing line means is implemented.

6. The processor as recited in one of the preceding claims,
wherein at least one memory unit is provided, designed for use as a stack, in particular being designed to indicate a stack underflow and/or overflow state, in particular of an operating system unit.